UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,304	12/03/2003	Chien-Te Chen	60417 (71987)	9698

7590 12/15/2005

Mr. Steven M. Jensen
Mr. Peter F. Corless
EDWARDS & ANGELL, LLP
101 Federal Street
Boston, MA 02110

EXAMINER	
NGUYEN, TUNG X	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/728,304	CHEN ET AL.
	Examiner	Art Unit
	Tung X. Nguyen	2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Pu et al. (u.s.p 6,646,349)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As to claim 1, Pu et al. disclose in Figs. 1-5, a chip carrier comprising: a core layer (10 of figure 5A) having a plurality of conductive traces (11, 12 of figure 5A, 7A) formed on at least one surface (surface of 100 figure 7A); the conductive traces comprising: at least one first trace (12 of figure 7A) connected with the passive component (15 of figure 7A) and having a first predetermined position (under 13 of figure 1) and two ends (first end connecting to 15 of figure 7A, second end connecting

to 19 of figure 7A), wherein the two ends are respectively electrically connected to a first bond finger (Z-shape of trace 12 of figure 7A) formed on the surface, mounted with the passive component (15 of figure 7A), and to a first ball pad (19 of figure 7A) formed on an opposite surface of the chip carrier (101 of figure 7A), wherein the first predetermined position and the first bond finger are located on the same side relative to the passive component (15 of figure 7A); and at least one second trace (trace connecting to 18 of figure 7A) free of connection with the passive component (15 of figure 7A) and having two ends (120 of figure 7A) and a second predetermined position (under 13 of figure 7A) located on the same surface as the first predetermined position (fig. 7A); wherein one of the ends of the second trace is electrically connected to a second ball pad (18 of figure 7A) located on the same surface as the first ball pad (18, 19 of figure 7A); and a solder mask layer (13 of figure 7A) applied over the conductive traces and formed with a plurality of openings (130, 131 of figure 1) for at least exposing the first predetermined position and the second predetermined position.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. (u.s.p 6,646,349); in view of Ogawa et al. (u.s.p 6,577,490).

As to claim 2-3, Pu et al. disclose in Figs. 1-7, all of the limitations and Pu et al. are silent about the device under test is resistor or inductor. However, It would have been obvious to a person having ordinary skill in the art at the time the invention to recognize the chip (DUT) including the resistors or inductors. For examble, Ogawa et al. disclose the same system as Pu et al. for testing device under test (DUT 160) is resistor or inductor.

As to claim 4, Pu et al. disclose in Figs. 1-7, all of the limitations except for each of the first predetermined position and the second predetermined position is at least formed with a nickel/gold (Ni/Au) layer. However, Ogawa et al. disclose (col. 11, lines 20-25) each of the first predetermined position and the second predetermined position is at least formed with a nickel/gold (Ni/Au) layer for good transmitting or receiving signal from the tester or DUT. Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention to modify the system of Pu et al., and provide the first and second predetermined position formed with a nickel/gold (Ni/Au) layer, as taught by Ogawa et al. for good transmitting or receiving signal from the tester or DUT.

As to claim 5, Ogawa et al. discloses the chip carrier (900 of figure 16) is a substrate (901 of figure 16).

As to claim 6, Ogawa et al. discloses the chip carrier, wherein the passive component (160 of figure 16) is serially connected to the first trace by means of surface mount technology (SMT).

As to claim 7, Ogawa et al. discloses the core layer (col. 2, lines 57-65) is made of a material selected from the group consisting of FR4 resin, glass resin, BT (bismaleimide triazine) resin, epoxy fesin, polyimide resin, and cyanide resin.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8, 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. (u.s.p 6,646,349); in view of Admitted Prior Art (heretoafter APA).

As to claim 8, Pu et al. disclose in Figs. 1-7, a chip carrier comprising (fig. 7A): a core layer (10 of figure 7A) having a plurality of conductive traces (11-12 of figure 7A) formed on at least one surface; the conductive traces (12 of figure 7A) comprising:

At least one first trace (12 of figure 7A) connected with the passive component (15 of figure 7A) and having a first predetermined position (under 13 of figure 7A) and two ends (110 connecting to 15 and connecting to 19 of figure 7A); wherein the two ends are respectively electrically connected to a first bond finger (first end of 12 connect to 15 of figure 7A) formed on the surface, mounted with the passive component (15); and to a first ball pad (19 of figure 7A) formed on an opposite surface of the chip carrier (101 of figure 7A); wherein the first predetermined position and the first bond finger are located on the same side relative to the passive component (fig. 7A); and

At least one second trace (trace connecting to 18 of figure 7A) free of connection with the passive component (15 of figure 7A) and having two ends and a second predetermined position (under 13 of figure 7A) located on the same surface as the first predetermined position (fig. 7A); wherein one of the ends of the second trace is electrically connected to a second ball pad (18 of figure 7A) located on the same surface as the first ball pad (19 of figure 7A); and

A solder mask layer (13 of figure 7A) applied over the conductive traces and formed with a plurality of openings (130, 131 of figure 1) for at least exposing the first predetermined position and the second predetermined position.

Pu et al. Do not disclose the two test heads respectively with the first ball pad and second ball pad, which are situated on the same surface of the chip carrier, to testing the electrical performance of the passive component.

However, APA disclose in Figs. two test heads respectively with the first ball pad (87 of figure 8) and second ball pad (85 of figure 8), which are situated on the same surface of the chip carrier, to testing the electrical performance of the passive component (81) for transmitting signal from the passive component to the tester. Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Pu et al. and provide the two test head, as taught by APA for transmitting signal from the passive component to the tester.

As to claim 11-12, Pu et al. disclose in Figs. 1-7, all of the limitations and Pu et al. are silent about the device under test is resistor or inductor. However, It would have been obvious to a person having ordinary skill in the art at the time the invention to

recognize the chip (DUT) including the resistors or inductors. For examble, Ogawa et al. disclose the same system as Pu et al. for testing device under test (DUT 160) is resistor or inductor.

As to claim 13, Pu et al. disclose in Figs. 1-7, all of the limitations except for each of the first predetermined position and the second predetermined position is at least formed with a nickel/gold (Ni/Au) layer. However, Ogawa et al. disclose (col. 11, lines 20-25) each of the first predetermined position and the second predetermined position is at least formed with a nickel/gold (Ni/Au) layer for good transmitting or receiving signal from the tester or DUT. Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention to modify the system of Pu et al., and provide the first and second predetermined position formed with a nickel/gold (Ni/Au) layer, as taught by Ogawa et al. for good transmitting or receiving signal from the tester or DUT.

As to claim 14, Ogawa et al. discloses the chip carrier (900 of figure 16) is a substrate (901 of figure 16).

As to claim 15, Ogawa et al. discloses the chip carrier, wherein the passive component (160 of figure 16) is serially connected to the first trace by means of surface mount technology (SMT).

As to claim 16, Ogawa et al. discloses the core layer (col. 2, lines 57-65) is made of a material selected from the group consisting of FR4 resin, glass resin, BT (bismaleimide triazine) resin, epoxy resin, polyimide resin, and cyanide resin.

As to claim 17, Ogawa et al. discloses all of the limitation except for the test head is a test probe (61 of figure 8) of a test system. However, APA disclose the test head (80 of figure 8) is a test probe (61 of figure 8) of a test system for transmitting the signal from the passive component to the tester. Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to of Ogawa et al., and provide the test head with a test probe, as taught by APA for transmitting the signal from the passive component to the tester.

6. Claims 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. (u.s.p 6,646,349); in view of Pedersen et al. (u.s.p 5,698,895).

As to claims 9-10, Pu et al. discloses all of the limitations except for the conductive jig made by conductive rubber or metal. However, Pedersen et al. disclose the conductive jig consider to be conductive fuse (50a of figure 2) for enabling the passive component tested on the same time (col. 10, lines 1-10). Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Ogawa et al., and provides the conductive jig, as taught by Pedersen et al. for enabling the passive component tested on the same time (col. 10, lines 1-10).

Response to Arguments

7. Applicant's arguments, see Remark on pages 3-5, filed 9/27/05, with respect to claims 1-17 have been fully considered and are persuasive. The last Office Action has been withdrawn.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X. Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN
12/05/05

VINH NGUYEN
PRIMARY EXAMINER
A.U. 2829
12/12/05